The documentation and process conversion measures necessary to comply with this revision shall be completed by 10 August 2004.

INCH-POUND

MIL-PRF-19500/396J
10 June 2004
SUPERSEDING
MIL-PRF-19500/396H
4 January 2002

* PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, SWITCHING,
TYPES 2N3762, 2N3762L, 2N3762U4, 2N3762UA, 2N3763, 2N3763L, 2N3763U4,
2N3763UA, 2N3764, AND, 2N3765,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

* This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP silicon switching transistors. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500 and two levels of product assurance are provided for each unencapsulated device type.

1.2 Physical dimensions. See figure 1, (2N3762L and 2N3763L (TO-5), 2N3762 and 2N3763 (TO-39), 2N3764 and 2N3765 (TO-46)), figure 2 (U4), figure 3 (UA), and figure 4 (die) herein.

* 1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Types	P_T T_A = +25°C (1)	P_T T_C = +25°C (1)	P_T $T_{SP(AM)}$ = +25°C (1)	P_T $T_{SP(IS)}$ = +25°C (1)	$R_{\theta JA}$ Steel (2)	$R_{\theta JA}$ Kovar (2)	$R_{\theta JC}$ Steel (2)	$R_{\theta JC}$ Kovar	$R_{\theta JSP}$ (AM) (2)	$R_{\theta JSP}$ (IS) (2)	T_J and T_{STG}
	W	W	W	W	°C/W	°C/W	°C/W	°C/W	°C/W	°C/W	°C
2N3762, L	1.0	2			175	175	30	50			-65 to +200
2N3762U4		10					15				-65 to +200
2N3762UA			5	1.94					35	90	-65 to +200
2N3763, L	1.0	2			175	175	30	50			-65 to +200
2N3763U4		10					15				-65 to +200
2N3763UA			5	1.94					35	90	-65 to +200
2N3764	0.5	2			325	350	70	60			-65 to +200
2N3765	0.5	2			325	350	70	60			-65 to +200

Types	V_{CBO}	V_{CEO}	V_{EBO}	I_C
	V dc	V dc	V dc	A dc
2N3762, L, 2N3762U4, 2N3762UA, 2N3764	40	40	5	1.5
2N3763, L, 2N3763U4, 2N3763UA, 2N3765	60	60	5	1.5

(1) For derating, see figures 5 through 11.
(2) For thermal curves, see figures 12 through 18.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://www.dodssp.daps.mil/.

1.4 Primary electrical characteristics T_A = +25°C. (Unless otherwise indicated, applies to all devices.).

Limits	h_{FE1} V_{CE} = 1.0 V dc; I_C = 10 mA dc	h_{FE3} V_{CE} = 1.0 V dc; I_C = 500 mA dc	h_{FE5} (1) V_{CE} = 5.0 V dc; I_C = 1.5 A dc	
			2N3762 2N3762L 2N3764	2N3763 2N3763L 2N3765
Min	35	40	30	20
Max		140		

Limits	$\|h_{FE}\|$ f = 100 MHz V_{CE} = 10 V dc I_C = 50 mA dc		$V_{CE(SAT)3}$ I_C = 500 mA dc I_B = 50 mA dc (1)	C_{obo} V_{CE} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	Pulse response			
					See figure 19		See figure 20	
	2N3762 2N3764	2N3763 2N3765	V dc	pF	t_d ns	t_r ns	t_s ns	t_f ns
Min	1.8	1.5						
Max	6.0	6.0	0.5	25	8	35	80	35

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

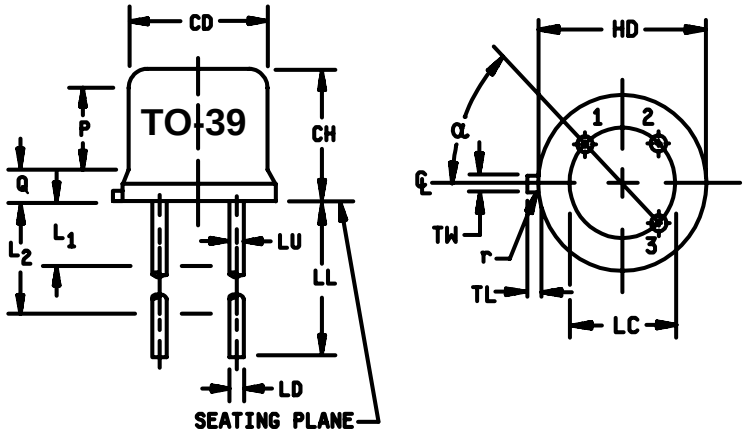
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

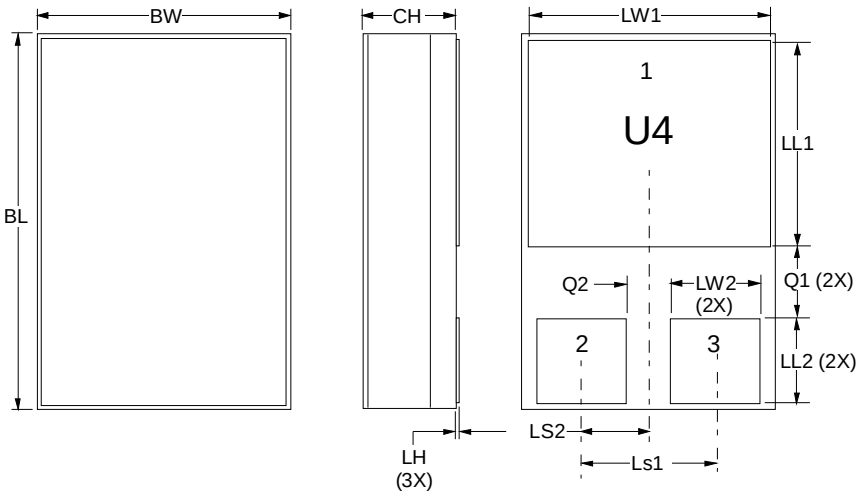


Symbol	TO-5, 39		TO-46		Notes
	Min	Max	Min	Max	
CD	.305	.355	0.178	0.195	
CH	.240	.260	0.065	0.085	
HD	.355	.370	0.209	0.230	
LC	.200 TP		0.100 TP		4
LD	.016	.021	0.016	0.021	4, 5
LL	See notes 4, 5, 6, 7				
LU	.016	.021	0.016	0.021	5
L1		.050		0.050	5
L2	.250		0.250		5
TL	.029	.045	0.028	0.048	2
TW	.028	.034	0.036	0.046	
P	.100				
Q		.040			3
r		.010		0.007	2
a	45° TP		45° TP		

NOTES:

1. Dimensions are in inches.
2. Dimension TL measured from maximum HD. Dimension r (radius) applies to both inside corners of tab.
3. Body contour optional within zone defined by HD, CD, and Q. Dimension P not applicable to TO-46.
4. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gauge and gauging procedure.
5. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
6. For TO-5 packages, dimension LL shall be 1.5 inches (38.1 mm) minimum and 1.75 inches (44.4 mm) maximum.
7. For TO-39 and TO-46 packages, dimension LL shall be 0.5 inch (12.7 mm) minimum and .75 inch (19.0 mm) maximum.
8. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
9. Lead 1 = emitter, lead 2 = base, lead 3 = collector (internally connected to the case).

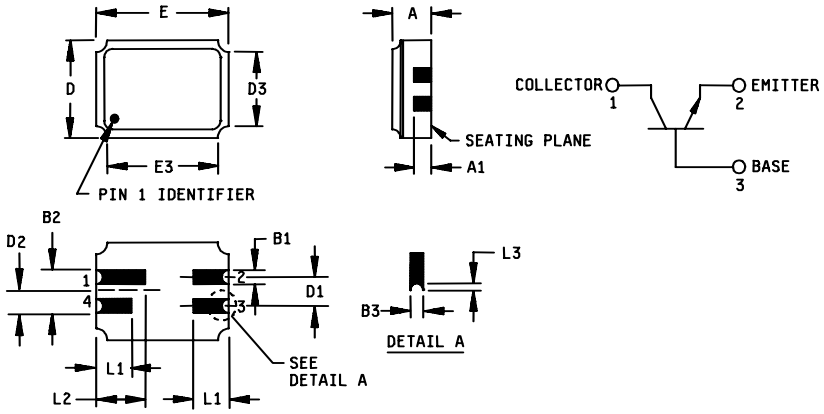
FIGURE 1. Physical dimensions (2N3762L and 2N3763L (TO-5), 2N3762 and 2N3763 (TO-39), 2N3764 and 2N3765 (TO-46)).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.049	.075	1.24	1.91
LH		.005		0.127
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.115	.125	2.92	3.18
LL2	.045	.055	1.14	1.40
LS1	.070	.095	1.78	2.41
LS2	.038	.048	.965	1.22
Q1	.045	.070	1.14	1.78
Q2	.025	.035	0.635	0.89
Terminal	BIPOLAR			
1	Collector			
2	Base			
3	Emitter			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

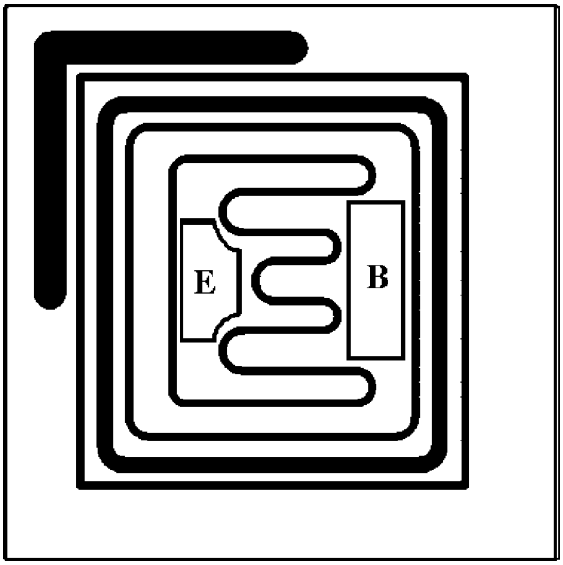
* FIGURE 2. Physical dimensions and configuration (U4).



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.061	.075	1.55	1.90	3
A1	.029	.041	0.74	1.04	
B1	.022	.028	0.56	0.71	
B2	.075 REF		1.91 REF		
B3	.006	.022	0.15	0.56	5
D	.145	.155	3.68	3.93	
D1	.045	.055	1.14	1.39	
D2	.0375 BSC		.952 BSC		
D3		.155		3.93	
E	.215	.225	5.46	5.71	
E3		.225		5.71	
L1	.032	.048	0.81	1.22	
L2	.072	.088	1.83	2.23	
L3	.003	.007	0.08	0.18	5

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "A" controls the overall package thickness. When a window lid is used, dimension "A" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions "B3" minimum and "L3" minimum and the appropriately castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions, surface mount (UA version).



NOTES:
1. Chip size ..... .040 (1.02 mm) x .040 inch (1.02 mm) ± .001 inch (0.03 mm).
2. Chip thickness ..... .010 ± .0015 inch.
3. Top metal ..... Aluminum 15,000Å minimum, 18,000Å nominal.
4. Back metal ..... A. Al/Ti/Ni/Ag 12kÅ/3kÅ/7kÅ/7kÅ min.,15kÅ/5kÅ/10kÅ/10kÅ nominal.
   B. Gold 2,500Å minimum, 3,000Å nominal.
   C. Eutectic Mount - No Gold.
5. Backside ..... Collector.
6. Bonding pad..... B = .006 (0.15 mm) x .008 inch (0.2 mm), E = .006 (0.15 mm) x .004 inch (0.1 mm).

FIGURE 4. JANHCA and JANKCA die dimensions.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1, 2, 3, and 4 herein.

3.4.1 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I.

3.7 Marking. Devices shall be marked in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and 6.3 herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX, JANTXV and JANS levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV level
1b	Required	Required (JANTXV only)
2	Optional	Optional
3a 3b (1) 3c	Required Not applicable Required method 3131 of MIL-STD-750. See 4.3.3.	Required Not applicable Required method 3131 of MIL-STD-750. See 4.3.3.
4	Required	Optional
5	Required	Not required
6	Not applicable	Not applicable
7a and 7b	Optional	Optional
8	Required	Not required
9	I_{CBO2}, h_{FE3} read and record	Not applicable
10	24 hours minimum	24 hours minimum
11	I_{CBO2}; h_{FE3}; ΔI_{CBO2} = 100 percent of initial value or 10 nA dc, whichever is greater. Δh_{FE3} = ±15 percent	I_{CBO2}; h_{FE3}
12	See 4.3.1 240 hours minimum	See 4.3.1
(2) 13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 10 nA dc, whichever is greater; Δh_{FE3} = ±15 percent	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 10 nA dc, whichever is greater; Δh_{FE3} = ±15 percent
14a and 14b	Required	Required
15 and 16	Required	Not required

(1) Thermal impedance may be performed any time after sealing provided temperature cycling is performed in accordance with MIL-PRF-19500, screen 3 prior to this thermal test.

(2) PDA = 5 percent for screen 13, applies to ΔI_{CBO2}, Δh_{FE3}, I_{CBO2} ,h_{FE3}. Thermal impedance ($Z_{\theta JX}$) is not required in screen 13.

* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10-30 V dc; power shall be applied to achieve the required junction temperature, T_J = +135°C minimum using a minimum power dissipation = 75 percent of maximum rated P_T (see 1.3). NOTE: No heat sink or forced air cooling on the devices shall be permitted. Power burn-in conditions for "L", "U4", and "UA" suffix devices are identical to their corresponding non-suffix devices.

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.3 Thermal impedance ($Z_{\theta JX}$ measurements). The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The $Z_{\theta JX}$ limit used in screen 3c of 4.3 shall comply with the thermal impedance graph on figures 12 through 18 (less than or equal to the curve value at the same t_H time) or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and group A2 inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2 herein).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1 herein. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein except for thermal impedance. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

* 4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Conditions
B4	1037	V_{CB} = 10 - 30 V dc.
B5	1027	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) V_{CB} = 10 V dc, $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). Option 1: 96 hours minimum, sample size in accordance with table VIa of MIL-PRF-19500 adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hrs minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve T_J = +225°C minimum.
B6	3131	$R_{\theta JA}$ for TO-5, UA, and UB. $R_{\theta JC}$ for U4.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action.

Step	Method	Condition
1	1039	Steady-state life: Test condition B, 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0.
2	1039	HTRB: Test condition A, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

4.4.3.1 Group C inspection, table VII (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E. (Does not apply to U4 and UA)
C6	1027	1,000 hours at V_{CB} = 10 V dc; T_J = +150°C min. External heating of the device under test to achieve T_J = +150°C minimum is allowed provided that a minimum of 75 percent of rated power is dissipated. No heat sink or forced-air cooling on device shall be permitted.

4.4.3.2 Group C inspection, table VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E. (Does not apply to U4 and UA)
C5	3131	Thermal resistance see figures 12 through 18 (only applies to $R_{\theta JA}$ for TO-39, TO-5 and $R_{\theta JC}$ for U4). See 4.3.3.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500, table II herein. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current 2N3762, L, U4, UA; 2N3764 2N3763, L, U4, UA; 2N3765	3036	Bias condition D V_{CB} = 20 V dc V_{CB} = 30 V dc	ΔI_{CB02} (1)	100 percent of initial value or ± 10 nA dc, whichever is greater.
2	Forward current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 150 mA dc; pulsed see 4.5.1	Δh_{FE2} (1)	± 25 percent change from initial reading.
3	Collector to emitter voltage (saturated)	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$\Delta V_{CE(SAT)3}$ (2)	± 50 mV dc change from previous measured value

(1) Devices which exceed the table I limits for this test shall not be accepted.
(2) Applies to JANS only.

* TABLE I. Group A inspection

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical inspection 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = + 250°C at t = 24 hours or T_A = + 300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification)	2075	n = 1 device, c = 0				
Subgroup 2						
* Thermal Impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Collector to base, cutoff current	3036	Bias condition D	I_{CBO1}		10	µA dc
2N3762, 2N3764		V_{CB} = 40 V dc				
2N3763, 2N3765		V_{CB} = 60 V dc				
Emitter to base, cutoff current	3061	Bias condition D. V_{EB} = 5 V dc	I_{EBO1}		10	µA dc
2N3762, 2N3764						
2N3763, 2N3765						
Breakdown voltage collector to emitter	3011	Bias condition D; I_C = 10 mA dc	$V_{(BR)CEO}$			V dc
2N3762, 2N3764				40		
2N3763, 2N3765				60		
Collector to base cutoff current	3036	Bias condition D	I_{CBO2}		100	nA dc
2N3762, 2N3764		V_{CB} = 20 V dc				
2N3763, 2N3765		V_{CB} = 30 V dc				

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Collector to emitter cutoff current	3041	Bias condition A; V_{EB} = 2.0 V dc	I_{CEX1}		100	nA dc
2N3762, 2N3764		V_{CE} = 20 V dc				
2N3763, 2N3765		V_{CE} = 30 V dc				
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 2.0 V dc	I_{EBO2}		200	nA dc
Forward - current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 10 mA dc	h_{FE1}	35		
Forward - current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 150 mA dc; pulsed (see 4.5.1)	h_{FE2}	40		
Forward - current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	h_{FE3}	40	140	
Forward - current transfer ratio	3076	V_{CE} = 1.5 V dc; I_C = 1.0 A dc; pulsed (see 4.5.1)	h_{FE4}			
2N3762, 2N3764				30	120	
2N3763, 2N3765				20	80	
Forward - current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 1.5 A dc; pulsed (see 4.5.1)	h_{FE5}			
2N3762, 2N3764				30		
2N3763, 2N3765				20		
Collector to emitter voltage (saturated)	3071	I_C = 10 mA dc; I_B = 1 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)1}$		0.10	V dc
Collector to emitter voltage (saturated)	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)2}$		0.22	V dc
Collector to emitter voltage (saturated)	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)3}$		0.50	V dc
Collector to emitter voltage (saturated)	3071	I_C = 1.0 A dc; I_B = 100 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)4}$		0.90	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = 10 mA dc; I_B = 1 mA dc	$V_{BE(SAT)1}$		0.80	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		1.0	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc, pulsed (see 4.5.1)	$V_{BE(SAT)3}$		1.2	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = 1.0 A dc; I_B = 100 mA dc, pulsed (see 4.5.1)	$V_{BE(SAT)4}$	.90	1.40	V dc

See footnotes at end of table.

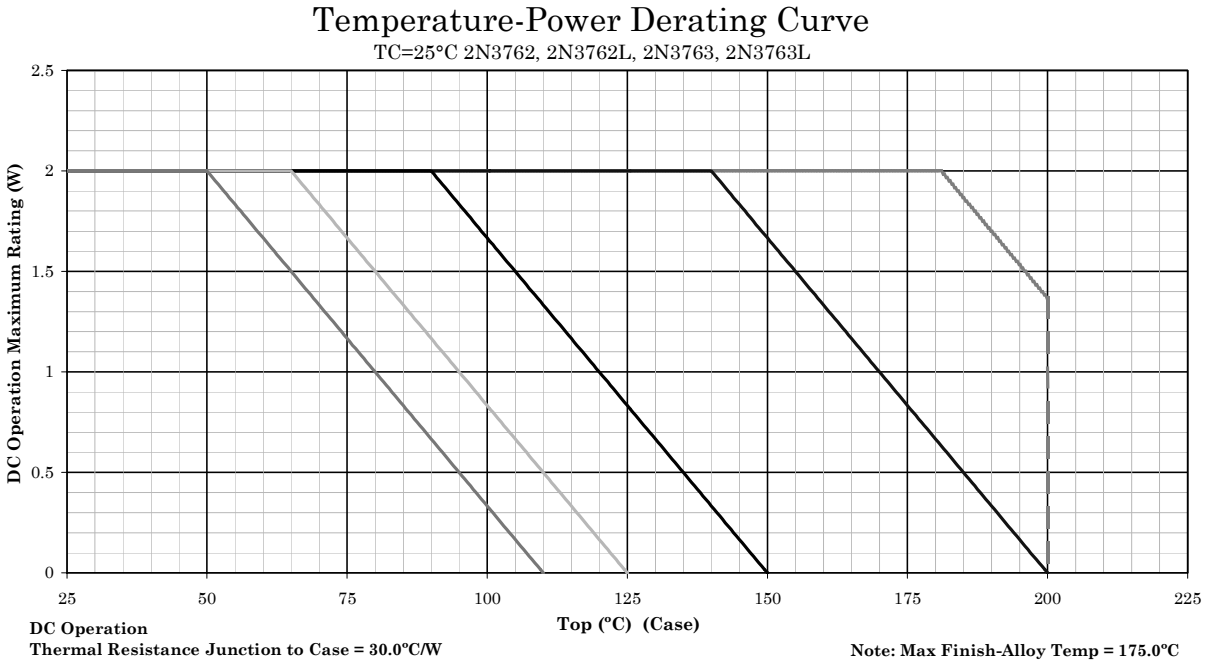
* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High-temperature operation		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A; V_{EB} = 2 V dc;	I_{CEX2}		150	µA dc
2N3762, 2N3764 2N3763, 2N3765		V_{CE} = 20 V dc; V_{CE} = 30 V dc				
Low-temperature operation		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	h_{FE6}	20		
Subgroup 4						
Magnitude of common emitter, small - signal short - circuit forward - current transfer ratio	3306	V_{CE} = 10 V dc; I_C = 50 mA dc; f = 100 MHz	$\|h_{fe}\|$			
2N3762, 2N3764 2N3763, 2N3765				1.8 1.5	6.0 6.0	
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		25	pF
Input capacitance (output open - circuited)	3240	V_{EB} = .5 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		80	pF
Pulse response						
Pulse delay time	3251	See figure 19	t_d		8	ns
Pulse rise time	3251	See figure 19	t_r		35	ns
Pulse storage time	3251	See figure 20	t_s		80	ns
Pulse fall time	3251	See figure 20	t_f		35	ns
Subgroups 5 and 6						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500. Electrical characteristics for "L", "U4", "and "UA" suffix devices are identical to their corresponding non-suffix devices.
2/ For resubmission of failed table I subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.

* TABLE II. Group E inspection (all quality levels) - for qualification only.

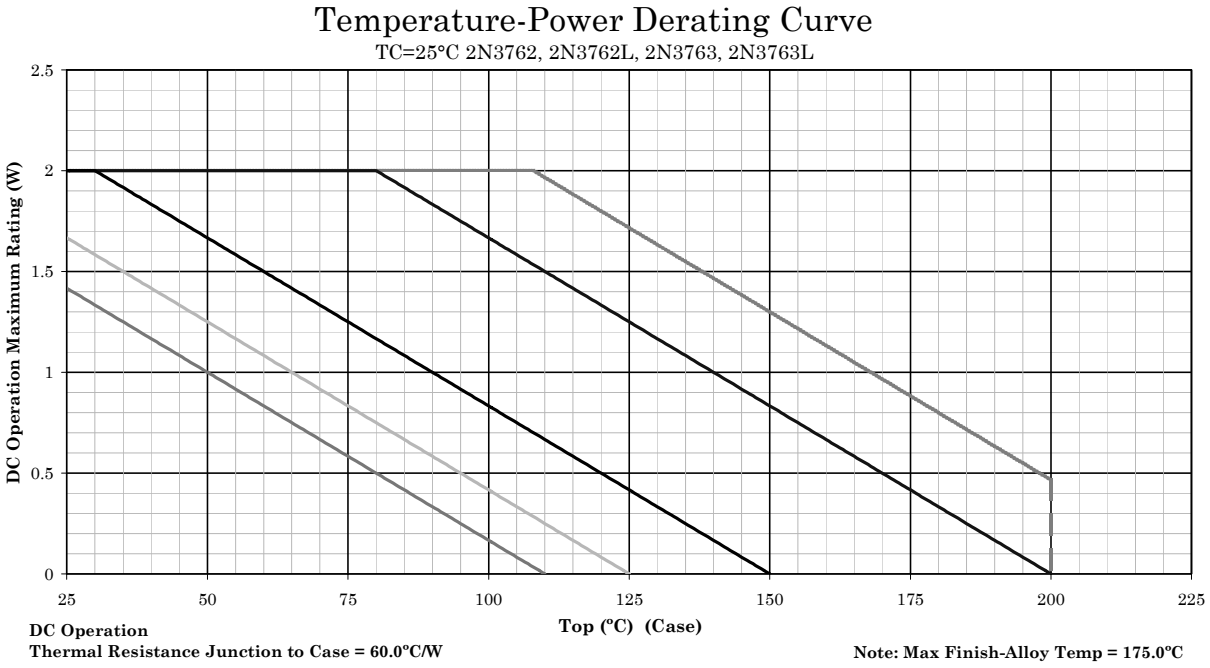
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices, c = 0.
Temperature cycling	1051	Test condition C, 500 cycles, sampling plan	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 2			45 devices, c = 0
Intermittent operating life	1037	V_{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 3			3 devices, c = 0
Destructive physical analysis Decap analysis only	2102		
Subgroup 4			
Thermal resistance	3131	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (can apply to multiple slash sheets). $R_{\theta JSP(AM)}$ need be calculated only.	15 devices, c = 0
Thermal impedance curves		Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	
Subgroup 5			
Not applicable.			
Subgroup 6			3 devices
ESD	1020		
Subgroup 8			45 devices, c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V dc. Condition B for devices < 400 Vd dc.	



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

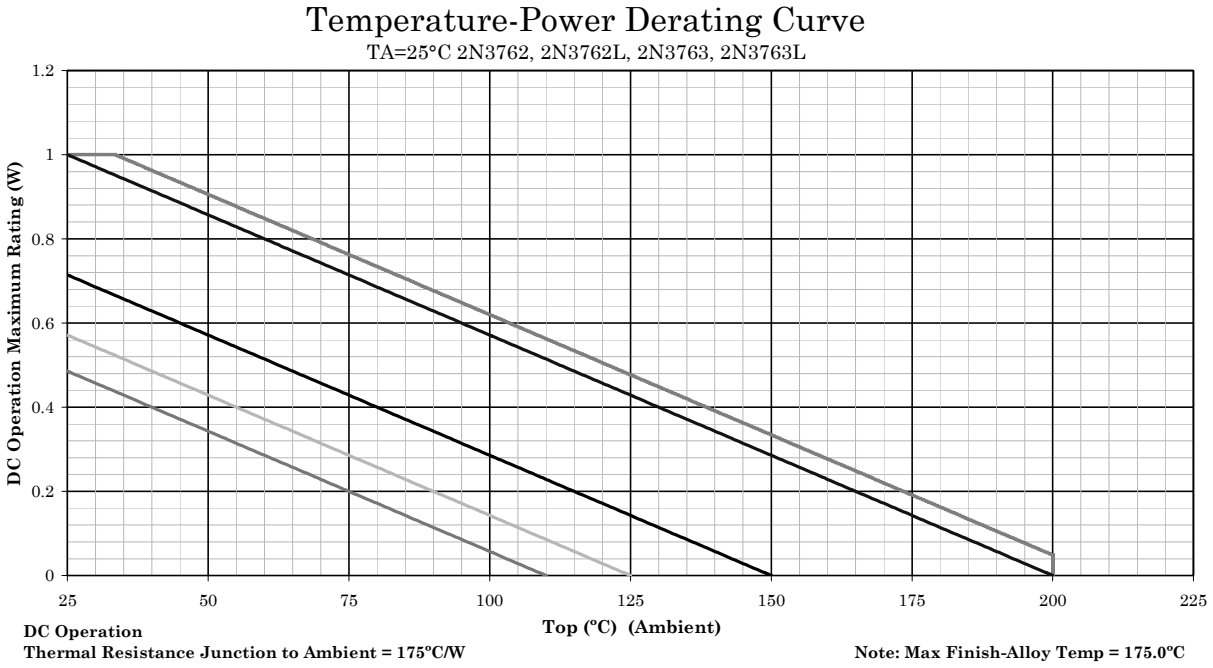
FIGURE 5a. Derating for Steel 2N3762L, 2N3763L(TO-5), and 2N3762, 2N3763(TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

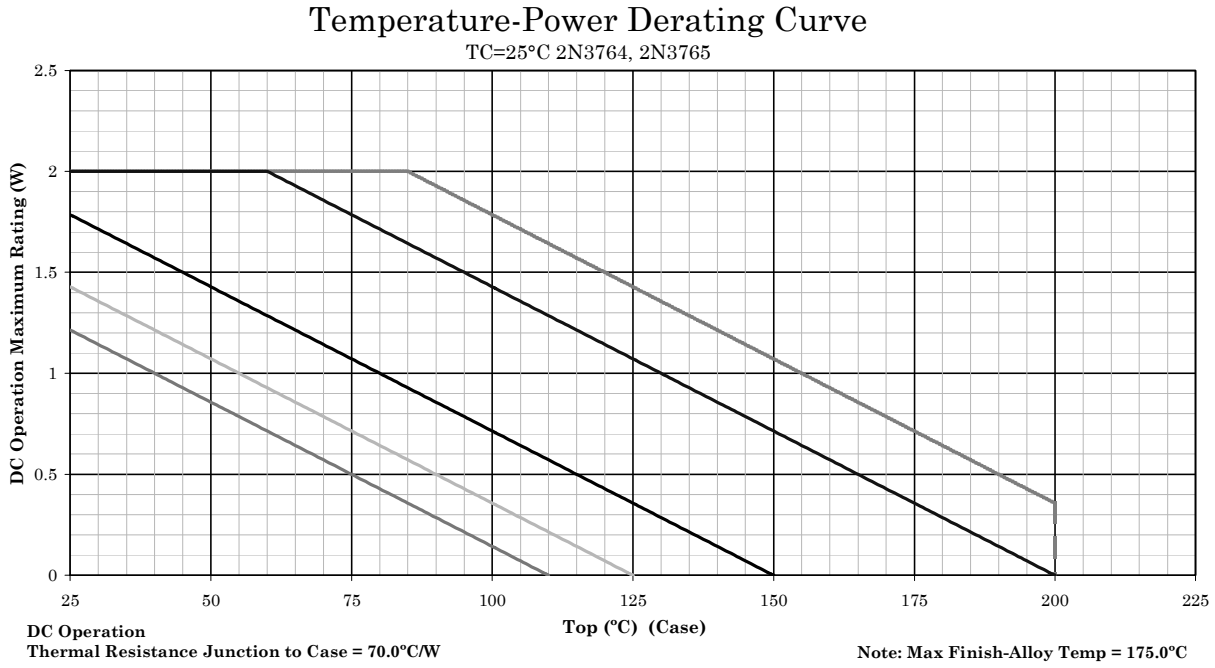
FIGURE 5b. Derating for Kovar 2N3762L, 2N3763L(TO-5), and 2N3762, 2N3763(TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

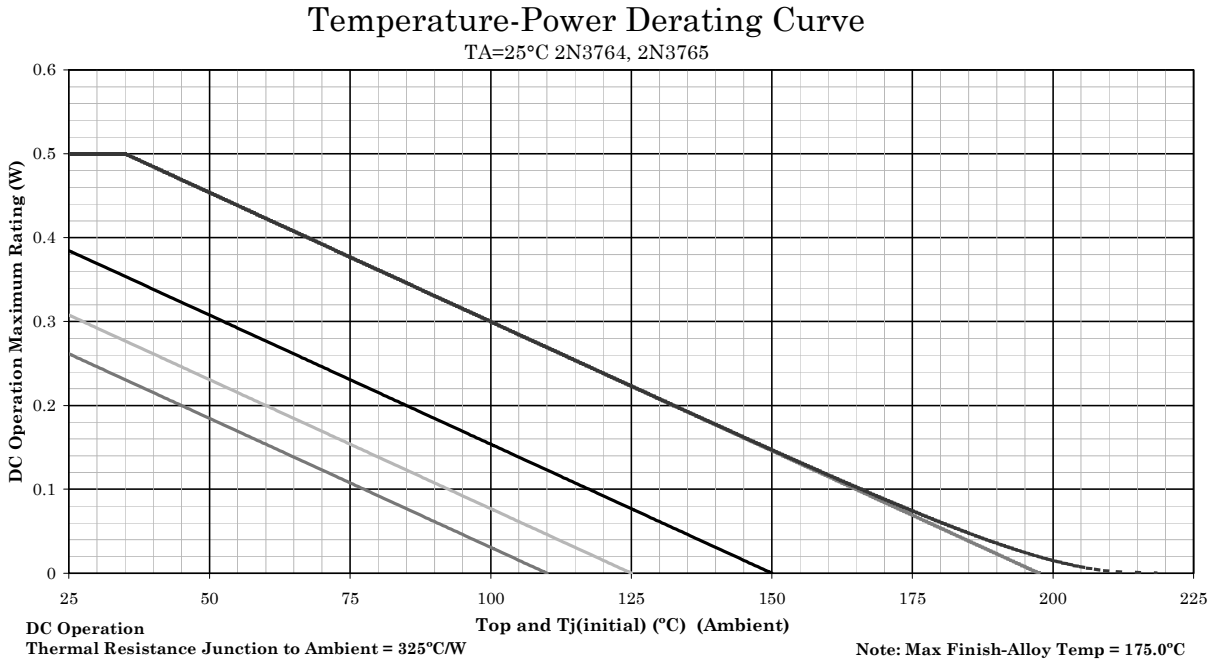
FIGURE 6. Derating for 2N3762L, 2N3763L(TO-5), and 2N3762, 2N3763(TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

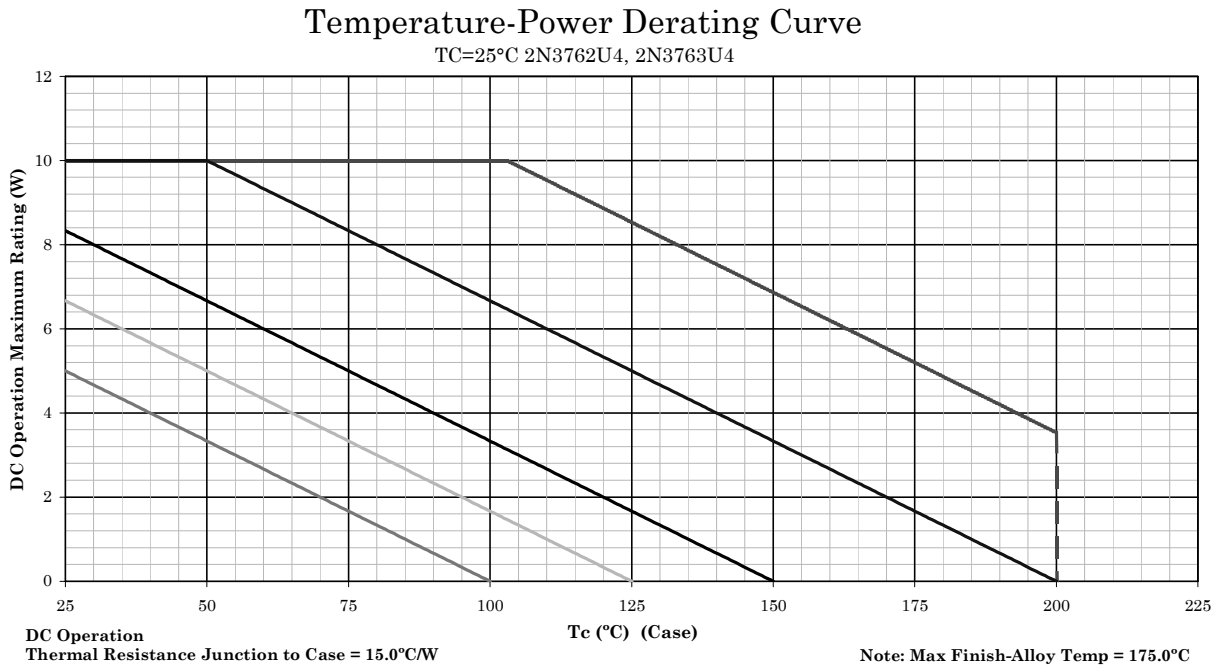
FIGURE 7. Derating for 2N3764, 2N3765 (TO-46).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
2. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
3. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

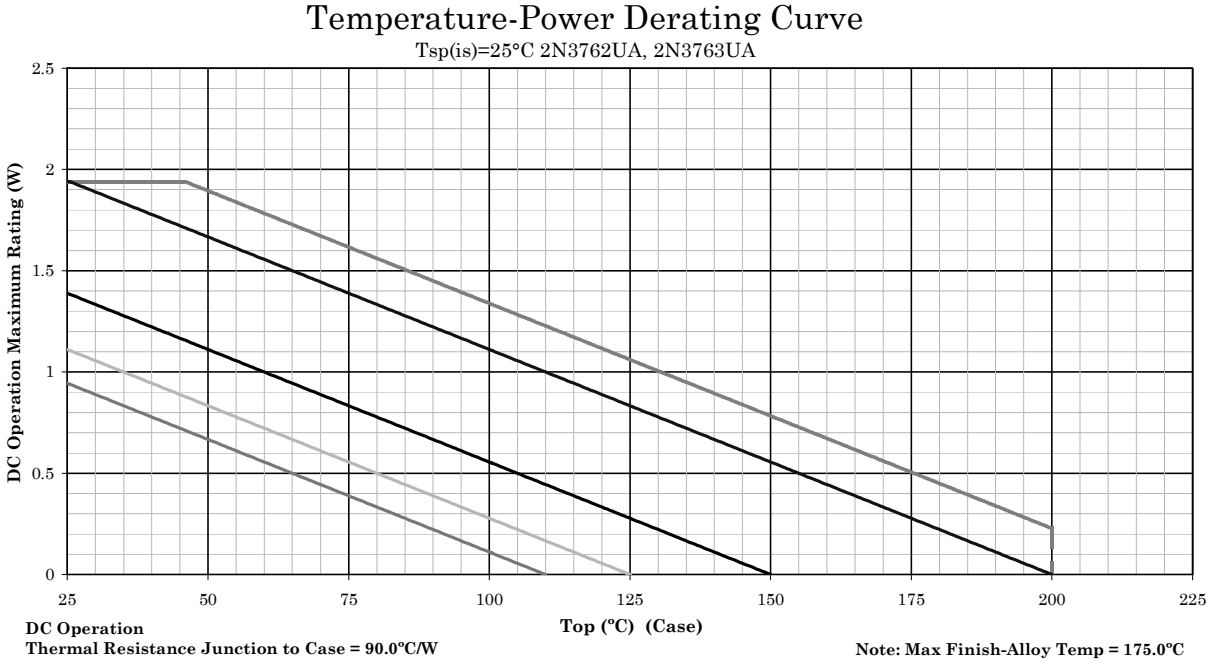
FIGURE 8. Derating for 2N3764, 2N3765(TO-46).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

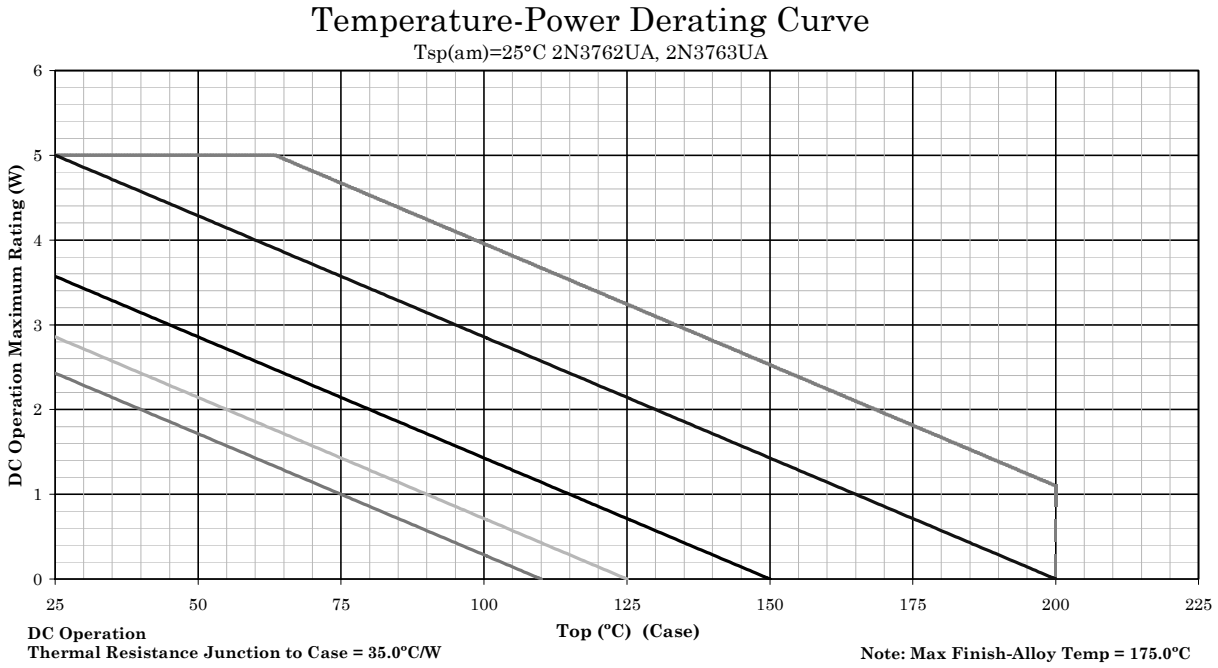
FIGURE 9. Derating for 2N3762U4, 2N3763U4.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 10. Derating for 2N3762UA, 2N3763UA.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 11. Derating for 2N3762UA, 2N3763UA.

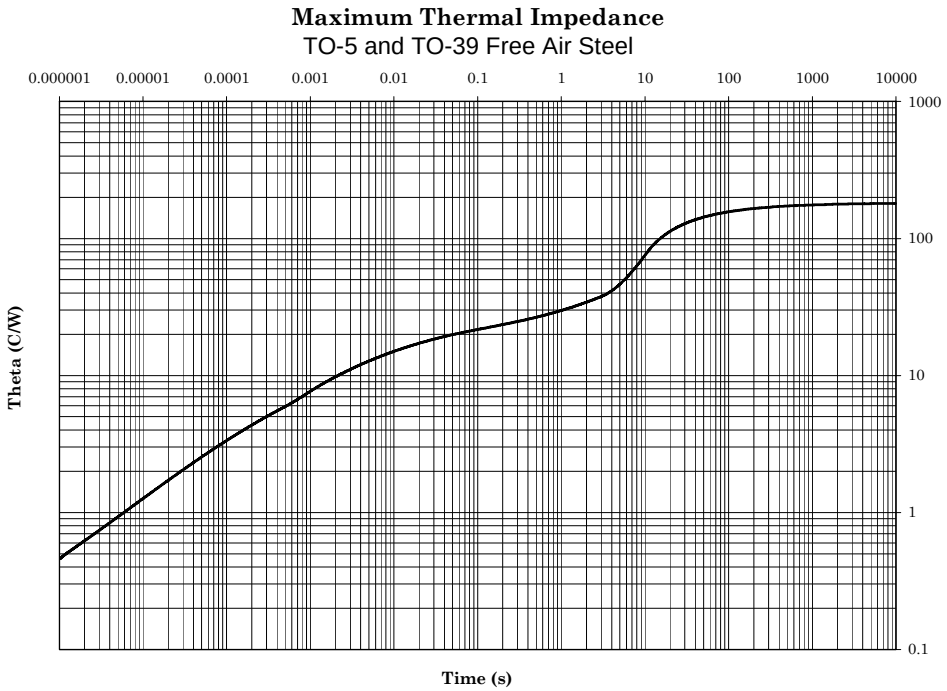


FIGURE 12. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

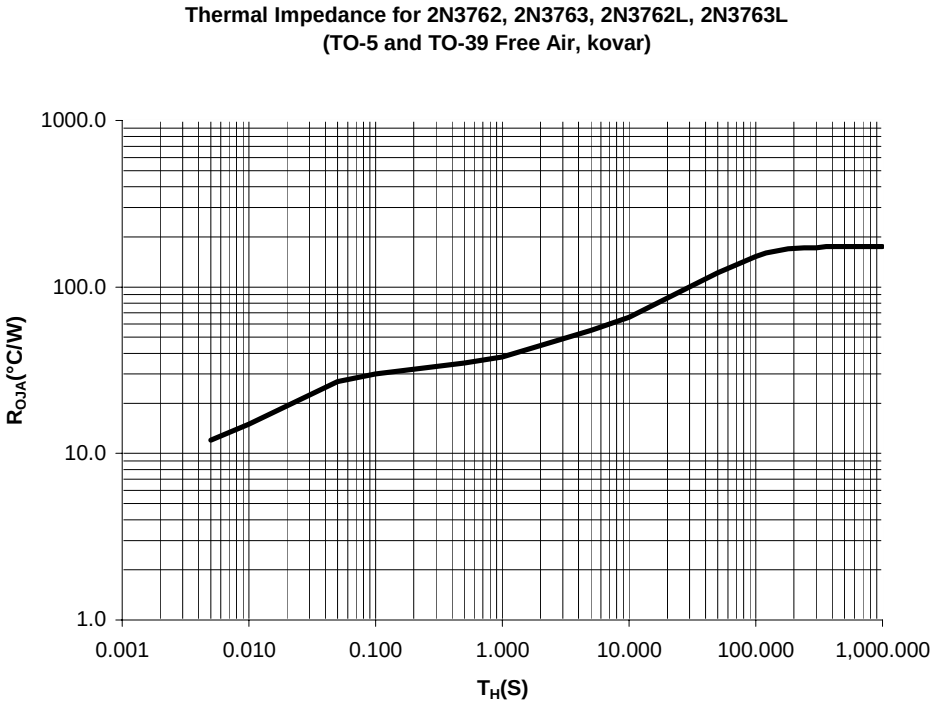


FIGURE 12a. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

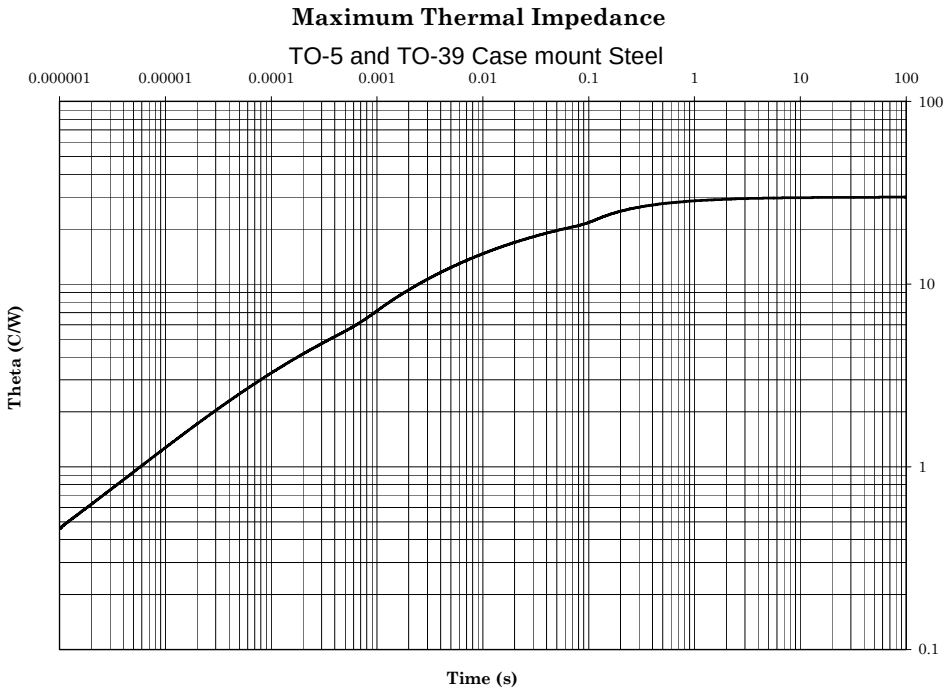


FIGURE 13. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

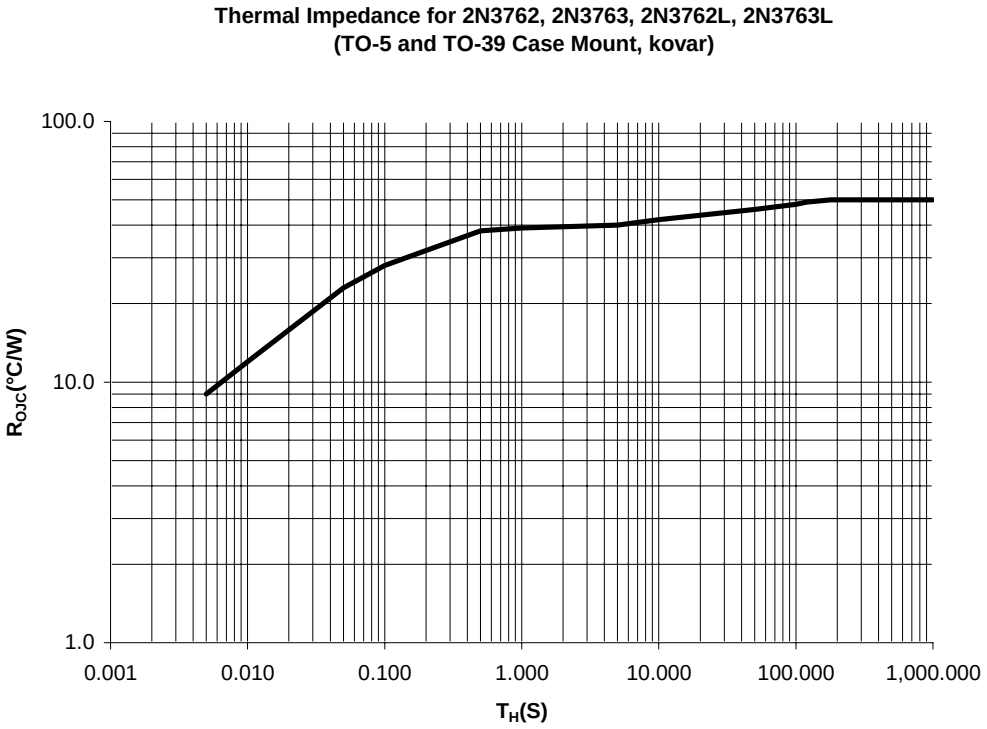


FIGURE 13a. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

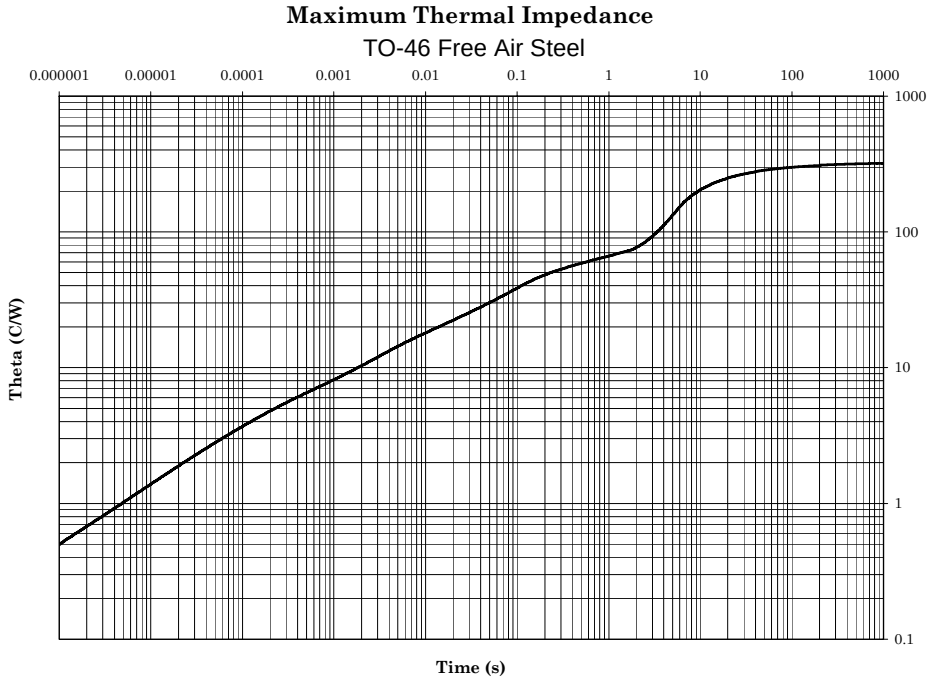


FIGURE 14. Thermal impedance for 2N3764, 2N3765 (TO-46).

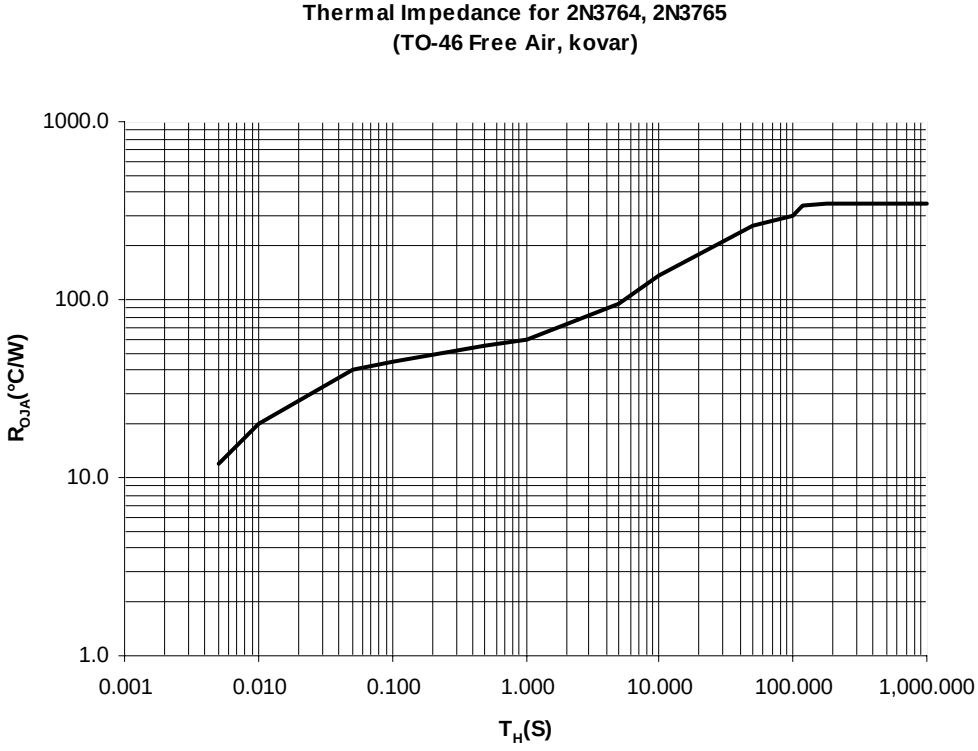


FIGURE 14a. Thermal impedance for 2N3764, 2N3765 (TO-46).

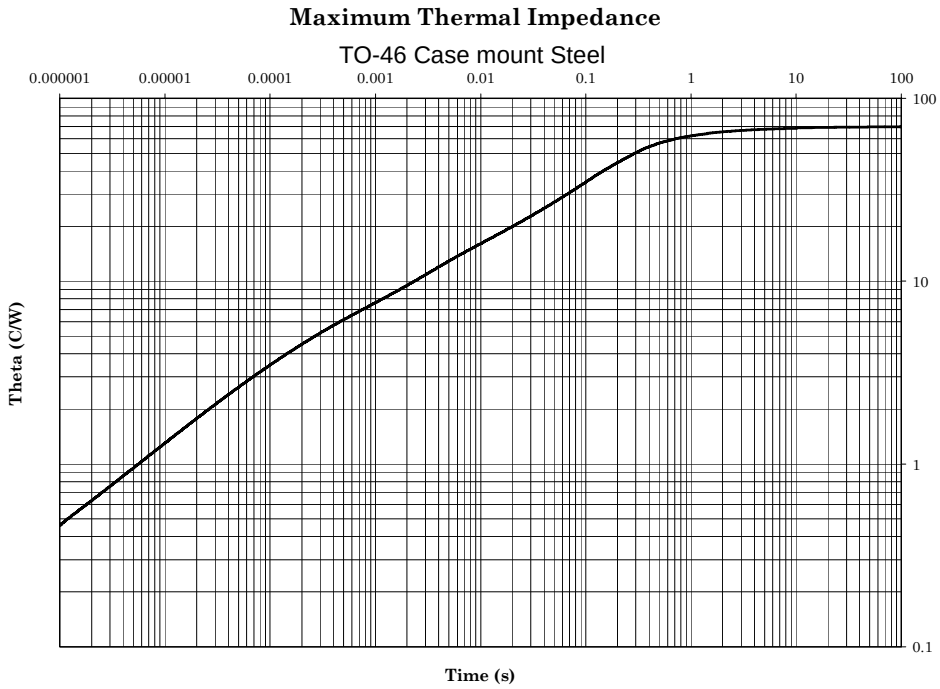


FIGURE 15. Thermal impedance for 2N3764, 2N3765 (TO-46).

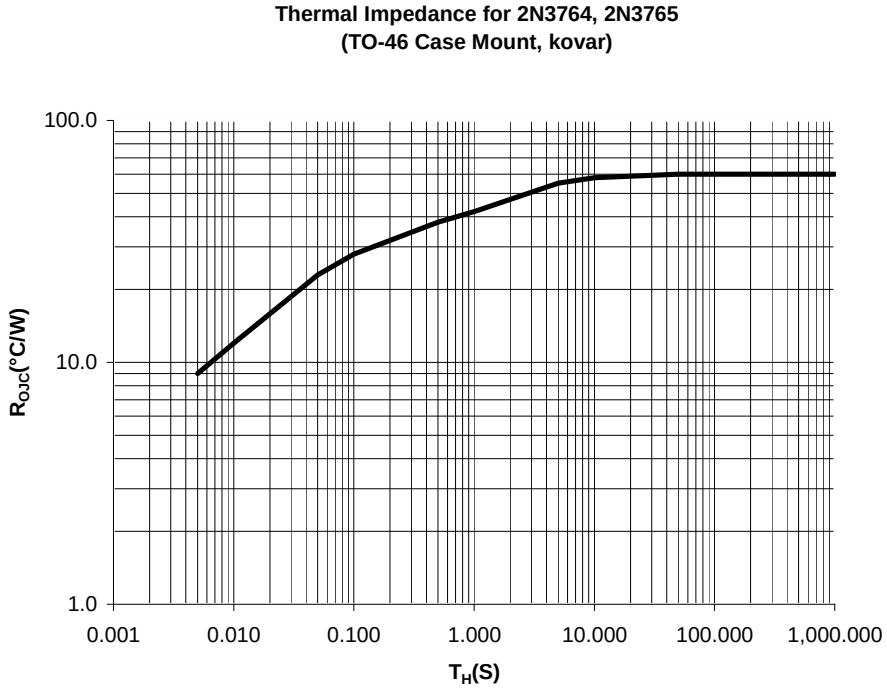


FIGURE 15. Thermal impedance for 2N3764, 2N3765 (TO-46).

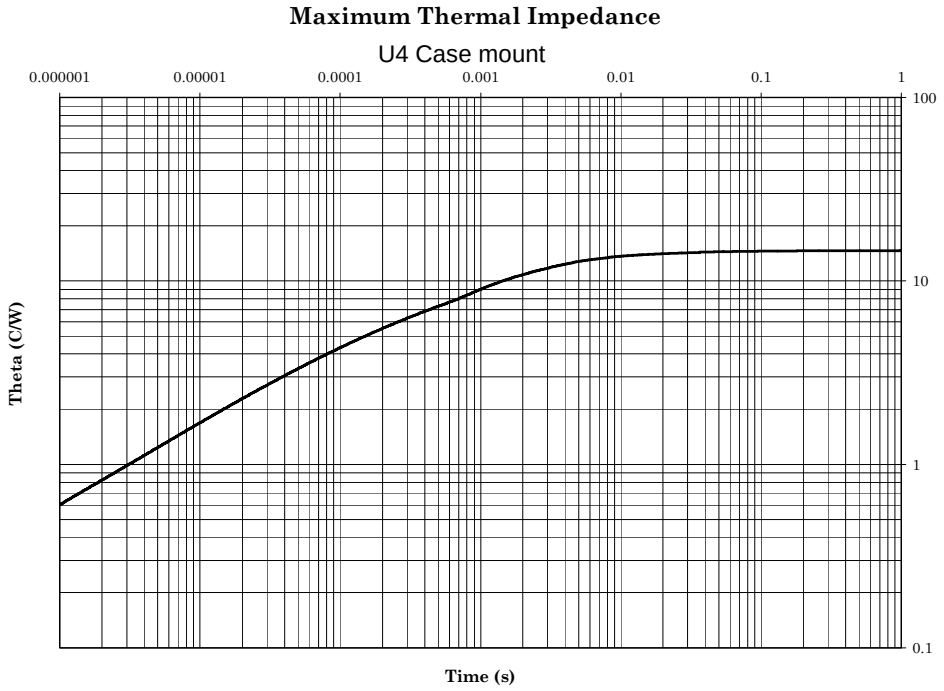


FIGURE 16. Thermal impedance for 2N3762U4, 2N3763U4 (U4).

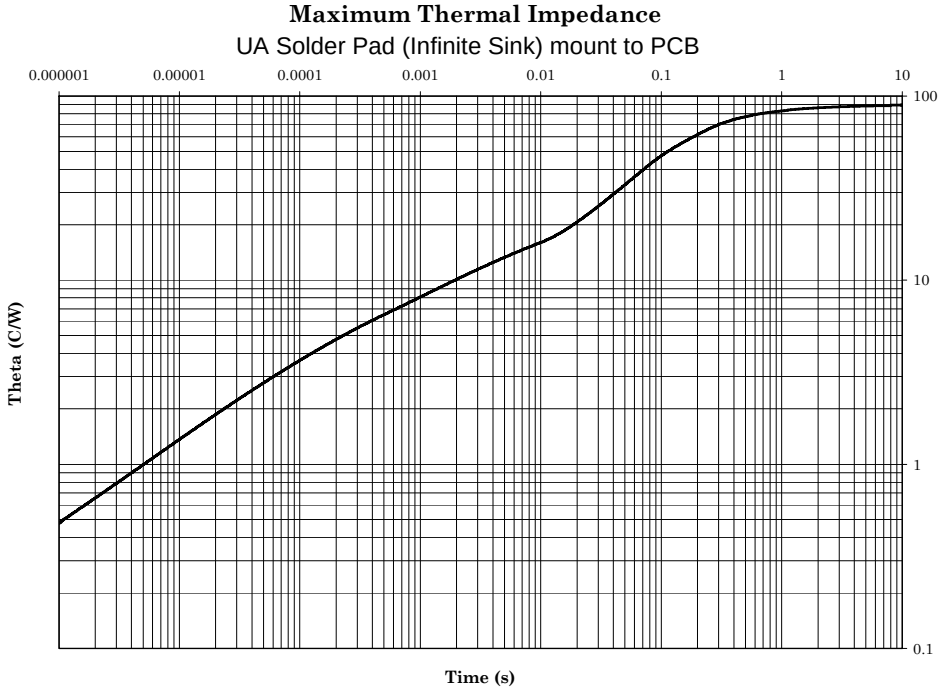


FIGURE 17. Thermal impedance for 2N3762UA, 2N3763UA (UA).

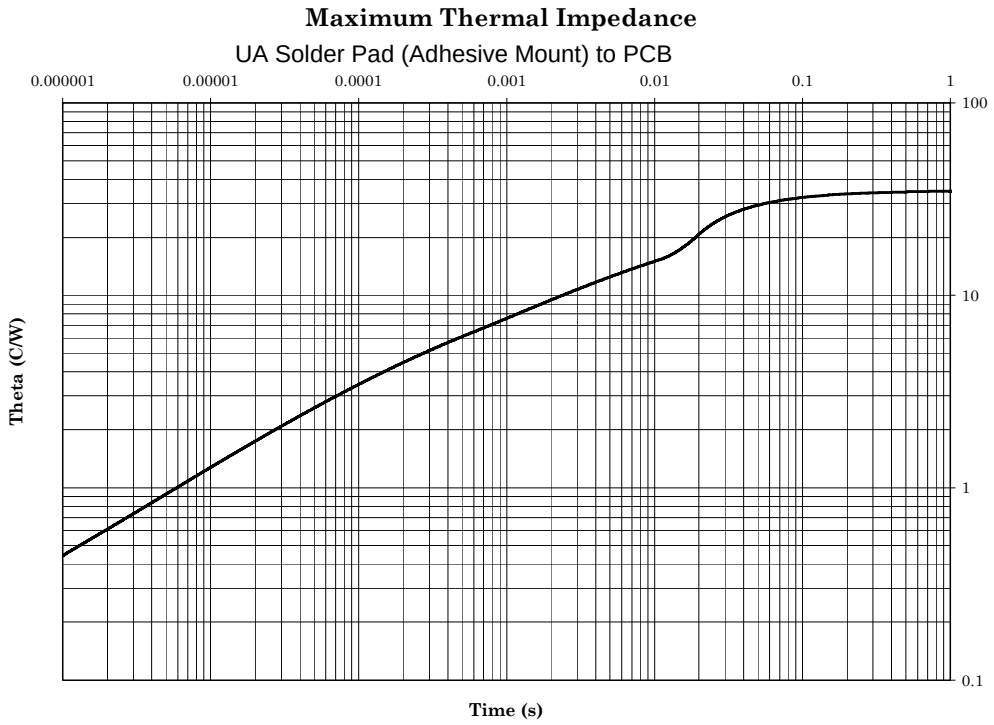
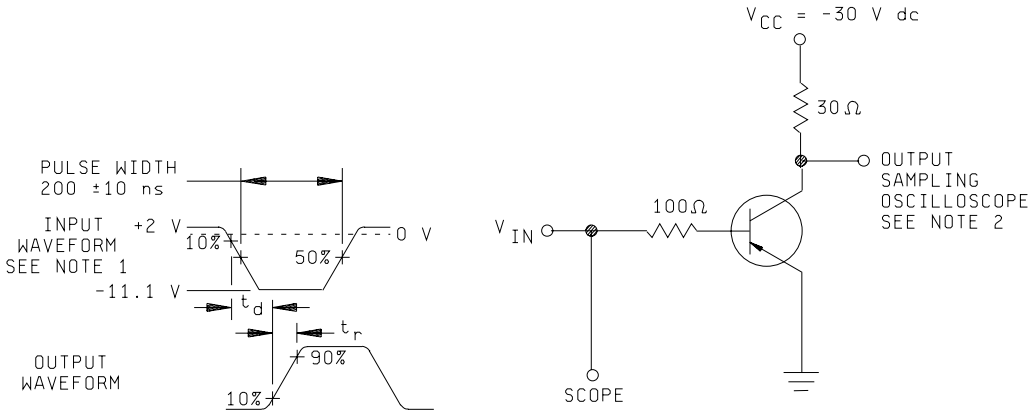
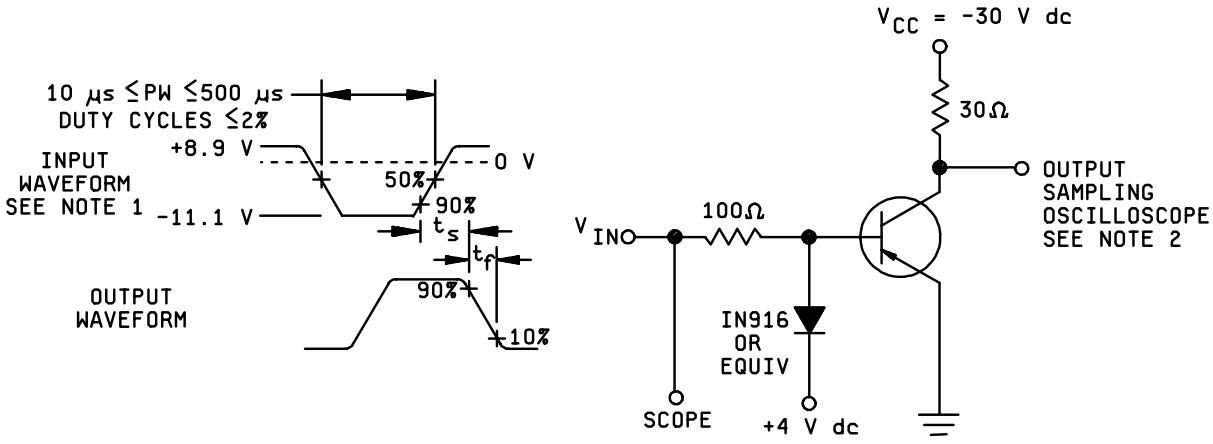


FIGURE 18. Thermal impedance for 2N3762UA, 2N3763UA (UA).



NOTES:
1. The rise time (t_r) of the applied pulse shall be ≤ 2 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω.
2. Sampling oscilloscope: Z_{in} ≥ 100 kΩ, C_{in} ≤ 12 pF, rise time ≤ .1 ns.
3. I_{B1} = -100 mA dc.

FIGURE 19. Pulse response test circuit for t_d and t_r.



NOTES:
1. The rise time (t_r) of the applied pulse shall be ≤ 2 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω.
2. Sampling oscilloscope: Z_{in} ≥ 100 kΩ, C_{in} ≤ 12 pF, rise time ≤ .1 ns.
3. I_{B1} = +I_{B2} = -100 mA dc.

FIGURE 20. Pulse response test circuit for t_s and t_f.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers' List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center Columbus, ATTN: DSCC-VQE, P. O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example, JANHCA2N2369A) will be identified on the QML.

JANC ordering information		
PIN	Manufacturer	
	43611	
2N3762	JANHCA2N3762	JANKCA2N3762
2N3763	JANHCA2N3763	JANKCA2N3763
2N3764	JANHCA2N3764	JANKCA2N3764
2N3765	JANHCA2N3765	JANKCA2N3765

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC
NASA - NA

Preparing activity:
DLA - CC

(Project 5961-2714)

Review activities:
Army - MI
Navy - AS, MC
Air Force - 19, 71, 99

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://www.dodssp.daps.mil.